Claims:

1   1.   A computer system having an interrupt handling apparatus, the computer system

2   comprising:

3   one or more processors;

4   one or more hardware devices that are capable of interrupting the one or more processors

5   using an interrupt signal;

6   an interrupt controller that is capable of handling the interrupts from the one or more

7   hardware devices and capable of independently generating a low priority interrupt signal and a

8   high priority interrupt signal for each processor;

9   the interrupt controller further comprising an enable device that is capable of enabling the

10   interrupt signal independently for each processor and a priority device that is capable of

11   assigning a priority to each interrupt signal destined for any processor wherein a particular

12   interrupt signal is capable of being routed to either processor and is capable of being assigned a

13   low priority or a high priority.

1   2.   The system of Claim 1, wherein the enable device further comprises a first

2   processor enable device that is capable of enabling the interrupt signals for the first processor and

3   a second processor enable device that is capable of enabling the interrupt signals for the second

4   processor.

1   3.   The system of Claim 2, wherein each enable device comprises one or more flip-

2   flips connected together with one or more logical gates.

1   4.   The system of Claim 3, wherein each enable device further comprises a register

2   containing an interrupt enable signal that is fed into the logical gates in order to enable the

3   interrupt signals of the particular processor.

1   5.   The system of Claim 1, wherein the priority device further comprises a first

2   processor priority device that is capable of assigning a priority to the interrupt signals for the first

3   processor and a second processor priority device that is capable of assigning a priority to the

4   interrupt signals for the second processor.

1   6.   The system of Claim 5, wherein each priority device comprises one or more flip-

2   flips connected together with one or more logical gates.

1   7.   The system of Claim 6, wherein each priority device further comprises a register

2   containing an interrupt priority signal that is fed into the logical gates in order to determine the

3   priority for the interrupt signals of the particular processor.

1   8.   The system of Claim 7, wherein each priority device selects between a low

2   priority signal and a high priority signal.

1   9.   The system of Claim 8, wherein the high priority signal comprises an FIQ signal

2   and the low priority signal comprises an IRQ signal.

1   10.   The system of Claim 1, wherein the interrupt controller further comprises a device

2   for multiplexing the one or more hardware interrupt signals with one or more software interrupt

3   signals so that the processors are capable of being interrupted by hardware devices and software.

1   11.   The system of Claim 10, wherein the software interrupt signals comprise a

2   software interrupt generated by one processor to interrupt another processor.

1   12.   A computer system having an interrupt handling apparatus, the computer system

2   comprising:

3   one or more processors;

4   one or more hardware devices that are capable of interrupting the one or more processors

5   using an interrupt signal;

6   an interrupt controller that is capable of handling the interrupts from the one or more

7   hardware devices and capable of independently generating a low priority interrupt signal and a

8   high priority interrupt signal for each processor;

9   the interrupt controller further comprising means for independently enabling the interrupt

10   signal for each processor and means for independently assigning a priority to each interrupt

11   signal destined for any processor wherein a particular interrupt signal is capable of being routed

12   to either processor and is capable of being assigned a low priority or a high priority.

1   13.   The system of Claim 12, wherein the enable means further comprises a first

2   processor enable device that is capable of enabling the interrupt signals for the first processor and

3   a second processor enable device that is capable of enabling the interrupt signals for the second

4   processor.

1   14.   The system of Claim 13, wherein each enable device comprises one or more flip-

2   flips connected together with one or more logical gates.

1   15.   The system of Claim 14, wherein each enable device further comprises a register

2   containing an interrupt enable signal that is fed into the logical gates in order to enable the

3   interrupt signals of the particular processor.

1   16.   The system of Claim 12, wherein the priority means further comprises a first

2   processor priority device that is capable of assigning a priority to the interrupt signals for the first

3   processor and a second processor priority device that is capable of assigning a priority to the

4   interrupt signals for the second processor.

1   17.   The system of Claim 16, wherein each priority device comprises one or more flip-

2   flips connected together with one or more logical gates.

1   18.   The system of Claim 17, wherein each priority device further comprises a register

2   containing an interrupt priority signal that is fed into the logical gates in order to determine the

3   priority for the interrupt signals of the particular processor.

1   19.   The system of Claim 18, wherein each priority device selects between a low

2   priority signal and a high priority signal.

1   20.   The system of Claim 19, wherein the high priority signal comprises an FIQ signal

2   and the low priority signal comprises an IRQ signal.

1   21.   The system of Claim 12, wherein the interrupt controller further comprises a

2   device for multiplexing the one or more hardware interrupt signals with one or more software

3   interrupt signals so that the processors are capable of being interrupted by hardware devices and

4   software.

1   22.   The system of Claim 21, wherein the software interrupt signals comprise a

2   software interrupt generated by one processor to interrupt another processor.

1   23.   A method for interrupt handling in a multiple processor system, the method

2   comprising:

3   assigning the interrupt signal to one of the multiple processors based on availability of

4   each processor;

5   assigning a priority level to the interrupt signal wherein the priority is selected from one

6   or more different priorities; and

7   routing the interrupt signal with the assigned priority level to the assigned processor.

1   24.   The method of Claim 23, wherein assigning the processor further comprises

2   reading a register to determine the assignment of the interrupt signal to a particular processor.

1   25.   The method of Claim 24, wherein the register reading further comprises reading

2   an enable register associated with each processor to determine the availability of each processor

3   to handle the interrupt signal.

1   26.   The method of Claim 23, wherein the routing further comprises splitting up the

2   servicing of the interrupt signal between the processors.

1   27.   The method of Claim 23, wherein the processor assigning further comprises

2   dynamically assigning the processor to handle a particular interrupt signal.

1   28.   The method of Claim 23, wherein assigning the priority further comprises reading

2   a priority register to determine the priority of the interrupt signal.

1   29.   The method of Claim 28, wherein the priority assigning further comprises

2   assigning a low priority to the interrupt signal and assigning a high priority to the interrupt

3   signal.

1   30.   The method of Claim 23, wherein the priority assigning further comprises

2   dynamically assigning the priority to the interrupt signal.

1   31.   A method for interrupt handling in a multiple processor system, the method

2   comprising:

3   assigning the interrupt signal to one of the multiple processors based on availability of

4   each processor; and

5   assigning a priority level to the interrupt signal wherein the priority is selected from one

6   or more different priorities.

1   32.   The method of Claim 31, wherein assigning the processor further comprises

2   reading a register to determine the assignment of the interrupt signal to a particular processor.

1   33.   The method of Claim 32, wherein the register reading further comprises reading

2   an enable register associated with each processor to determine the availability of each processor

3   to handle the interrupt signal.

1   34.   The method of Claim 31, wherein the routing further comprises splitting up the

2   servicing of the interrupt signal between the processors.

1   35.   The method of Claim 31, wherein the processor assigning further comprises

2   dynamically assigning the processor to handle a particular interrupt signal.

1   36.   The method of Claim 31, wherein assigning the priority further comprises reading

2   a priority register to determine the priority of the interrupt signal.

1   37.   The method of Claim 36, wherein the priority assigning further comprises

2   assigning a low priority to the interrupt signal and assigning a high priority to the interrupt

3   signal.

1   38.   The method of Claim 31, wherein the priority assigning further comprises

2   dynamically assigning the priority to the interrupt signal.

1   39.   A computer system, comprising:

2   a first processor;

3   a second processor;

4   a peripheral controller having a first bus that is capable of connecting the first processor

5   to a set of peripheral resources and a second bus that is capable of connecting the second

6   processor to the same set of peripheral resources wherein each peripheral in the set of peripheral

7   resources is capable of generating an interrupt signal;

8   the peripheral controller further comprising an interrupt controller that is capable of

9   handling the interrupts from the set of peripheral resources and software interrupts and capable of

10   independently generating a low priority interrupt signal and a high priority interrupt signal for

11   each processor from the peripheral and software interrupts, the interrupt controller further

12   comprising a first processor enable device that is capable of enabling the interrupt signals for the

13   first processor, a second processor enable device that is capable of enabling the interrupt signals

14   for the second processor, a first processor priority device that is capable of assigning a priority to

15   the interrupt signals for the first processor and a second processor priority device that is capable

16   of assigning a priority to the interrupt signals for the second processor wherein a particular

17   interrupt signal is capable of being routed to either processor and is capable of being assigned a

18   low priority or a high priority.

1   40.   A computer system, comprising:

2   a first processor;

3   a second processor;

4   a peripheral controller comprising first communications means that is capable of

5   connecting the first processor to a set of peripheral resources and a second communications

6   means that is capable of connecting the second processor to the same set of peripheral resources

7   wherein each peripheral in the set of peripheral resources is capable of generating an interrupt

8   signal;

9   the peripheral controller further comprising an interrupt controller that is capable of

10   handling the interrupts from the set of peripheral resources and software interrupts and capable of

11   independently generating a low priority interrupt signal and a high priority interrupt signal for

12   each processor from the peripheral and software interrupts, the interrupt controller further

13   comprising means for enabling the interrupt signals for the first processor, means for enabling

14   the interrupt signals for the second processor, means for assigning a priority to the interrupt

15   signals for the first processor and means for assigning a priority to the interrupt signals for the

16   second processor wherein a particular interrupt signal is capable of being routed to either

17   processor and is capable of being assigned a low priority or a high priority.